REMARKS

Claims 1, 7, 12, 18, 22 and 27 are amended. Claims 1, 3-12, 14-22, 24-32 are pending. No new matter is added.

Prior Art Rejections under 35 U.S.C. Section 103

In the Office Action, claims 1, 5-7, 12, 16-18, 22, and 26-27 were rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over U.S. Patent 6,732,246 to Pickreign et. al. (Pickreign) in view of U.S. Patent 6,647,469 to Sharma et. al (Sharma). Applicant respectively traverses this rejection.

Claim 1 of the application recites, in part, a method that includes allocating space in a host memory for use as a buffer and accessing the contents of the buffer in response to a request for information in a network interface controller. Independent claims 7, 12, 18, 22 and 27 recite similar features.

An example of accessing the contents of the buffer is discussed in connection with FIG. 2 of the specification. In that example, when there is a call to read the EEPROM 15 by an application 52 on the host memory 30 via the driver for the first time after PHY initialization, the EEPROM buffer 35 is initialized. The entire contents of the EEPROM 15 are copied into the EEPROM buffer 35... Subsequent requests to read the EEPROM 15 by an application can be directed to the EEPROM buffer 35, thereby allowing the requested information to be accessed efficiently. (Specification, page 6, lines 1-14)

The Pickreign reference relates to *mapping* a host computer address space into a network interface adapter (NIA) address space. Although the reference discusses transferring data images stored in a NIA to a host computer, it does not teach accessing the contents of a buffer in response to a request for information in a network interface controller as recited in pending claim 1. Instead, the Pickreign reference discloses, in connection with FIG. 1, that:

> [I]n the case of a read operation, the NIA processor translates the host address as described herein, retrieves the data from the [sic.] NIA memory, such as the flash

> RAM, at the location(s) specified by the translated address(es) and writes the data into the data transfer registers for transmittal to the host computer.

(Pickreign, col. 4, lines 5-10)

Hence, when the NIA processor is notified that the host computer is requesting to read data from an address within the host computer address space assigned to the NIA, the NIA processor *translates* that address to an address *within* the NIA memory and writes the data to transfer registers for *transmittal* to the host computer. There is no teaching or suggestion of accessing the contents of the buffer in response to a request for information in a network interface controller as recited in pending claim 1.

The Office action acknowledges that the Pickreign reference does not expressly teach updating the contents of the network interface controller memory and correspondingly updating the contents of the buffer but alleges that the Sharma et. al. reference teaches a method of updating the contents of the network interface controller and correspondingly updating the contents of the buffer and that one would have been motivated to combine these references. Applicant respectively disagrees.

First, the Sharma reference relates to using read current transactions for improved performance in directory-based coherent I/O systems. As discussed in the summary section of the patent, a memory controller is disclosed that ensures data stored by agents are coherent with data stored in memory (Sharma, col. 5, lines 11-17). Although the Sharma reference discusses a coherent mode of operation, the disclosed method is very different from the subject matter of the pending claims. In particular, the reference discloses the coherent mode of operation as follows:

> In the coherent mode, the memory controller ensures that an agent's cache reflects the most up to date data. Using, for example, a MESI type protocol, the memory controller limits access to memory so that only one "owner" gets the cache line at any time for write access and that, during the extension of these write privileges, no other agent has a valid copy of the data subject to being updated. Thus, the memory controller

> implements a first set of rule in the coherent mode of operation to insure that all copies of data stored by the agents are coherent with data stored in the memory.

(Col. 3, line 62 – col. 4, line 5)

There is no teaching or suggestion of modifying the contents of the network interface controller memory and correspondingly modifying the contents of a host buffer memory as recited in the pending claims.

Second, one of ordinary skill in the art would not have been motivated to combine the Sharma reference with the Pickreign reference to obtain the subject matter of the pending claims. The Pickreign reference addresses problems relating to bottlenecking that occurs when data is transferred from a network interface adapter (NIA) to a host computer. (Pickreign, col. 1, lines 28-38) The Sharma reference addresses problems relating to improving usable bandwidth and the presence of "ping-ponging" which may occur between *contending* caches. (Sharma, col. 3, lines 47-51) The latter issue has nothing to do with what is addressed in the Pickreign reference.

At least for the foregoing reasons, it is clear that one of ordinary skill in the art would not have been motivated to combine the Pickreign and Sharma references to obtain the subject matter of any of independent claims 1, 7, 12, 18, 22 and 27. In view of the foregoing remarks, applicant respectfully requests reconsideration and withdrawal of the rejection of independent claims 1, 7, 12, 18, 22 and 27. Dependent claims 3-6, 8-11, 14-17, 19-21, 24-26 and 28-32 should be allowed at least for the same reasons.

In the Office Action, claims 3-4, 8-11, 14-15, 19-21, 24-25, and 28-29 were rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over the Pickreign reference in view of U.S. Patent 6,647,469 to Shah et. al (Shah).

Applicant respectfully disagrees. The prior remarks regarding the Pickreign reference are applicable and the Shah reference does not contain the features missing from the Pickreign reference.

The Shah reference relates to methods and systems for handling network and I/O communications. The Office Action alleges that the Shah reference discloses a method comprising initializing a device driver in a NDIS environment to allocate space in a host memory in less than a second and refers to the following statement in Shah:

> In addition, as previously described with reference to FIG. 2, in one embodiment, the present invention can provide additional fail-over paths to backup NIC adapters used for local host-to-host communications. In one embodiment, the network driver is adapter-type independent and supports multiple Ethernet emulations through multiple enhanced miniport drivers simultaneously.

(Shah, col. 7, lines 11-17)

The quoted section of Shah relates to supporting multiple Ethernet emulations through multiple enhanced miniport drivers simultaneously. There is no suggestion or teaching of initializing a device driver in a Network Device Driver Interface environment to allocate space in the host memory in less than a second as recited in pending claims 3, 9, 14, 19, 24 and 28. The Shah reference does not contain the features missing from the Pickreign reference. In view of the foregoing remarks, applicant respectfully requests reconsideration and withdrawal of the rejection of claims 3-4, 8-11, 14-15, 19-21, 24-25, and 28-29.

Claims 30-32 were rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over the Pickreign reference in view of the Sharma reference in view of the Shah reference. The Shah reference, however, does not disclose or suggest the claim features missing from the Pickreign and Sharma references. For at least these reasons, applicant respectively requests withdrawal of the rejection of claims 30-32 as well.

Conclusion

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Please apply any charges or credits to deposit account 06-1050, referencing Attorney Docket No. 10559-386001.

Respectfully submitted,

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